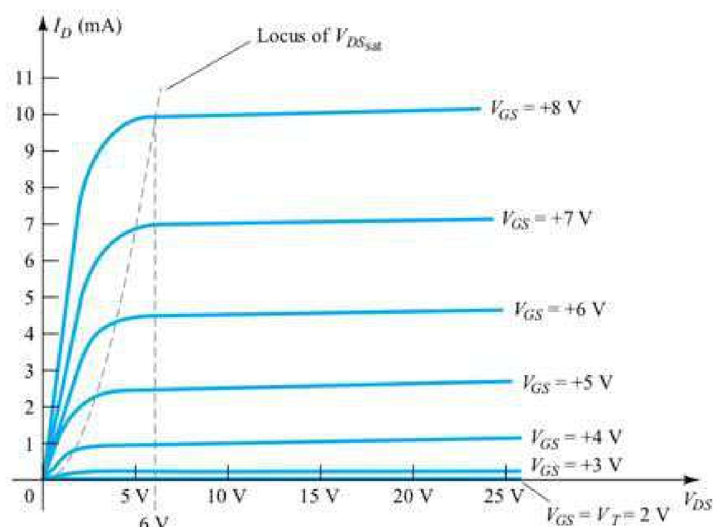

Figure 5.34 Drain characteristics of an *n*-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

For the characteristics of Fig. 5.33 the level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA. In general, therefore:

For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

Figure 5.34 clearly reveals that as the level of V_{GS} increased from V_T to 8 V, the resulting saturation level for I_D also increased from a level of 0 to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increased as the magnitude of V_{GS} increased, resulting in ever-increasing increments in drain current.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2 \tag{5.13}$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (5.13)] where $I_{D(\text{on})}$ and $V_{GS(\text{on})}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_T)^2} \tag{5.14}$$

Substituting $I_{D(\text{on})} = 10$ mA when $V_{GS(\text{on})} = 8$ V from the characteristics of Fig. 5.34 yields

$$k = \frac{10 \text{ mA}}{(8 \text{ V} - 2 \text{ V})^2} = \frac{10 \text{ mA}}{(6 \text{ V})^2} = \frac{10 \text{ mA}}{36 \text{ V}^2}$$
$$= \mathbf{0.278 \times 10^{-3} \ A/V^2}$$

and a general equation for I_D for the characteristics of Fig. 5.34 results in:

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2 \text{ V})^2$$

Substituting $V_{GS} = 4$ V, we find that

$$I_D = 0.278 \times 10^{-3}(4\text{ V} - 2\text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$
$$= 0.278 \times 10^{-3}(4) = \mathbf{1.11\ mA}$$

as verified by Fig. 5.34. At $V_{GS} = V_T$, the squared term is 0 and $I_D = 0$ mA.

For the dc analysis of enhancement-type MOSFETs to appear in Chapter 6, the transfer characteristics will again be the characteristics to be employed in the graphical solution. In Fig. 5.35 the drain and transfer characteristics have been set side by side to describe the transfer process from one to the other. Essentially, it proceeds as introduced earlier for the JFET and depletion-type MOSFETs. In this case, however, it must be remembered that the drain current is 0 mA for $V_{GS} \leq V_T$. At this point a measurable current will result for I_D and will increase as defined by Eq. (5.13). Note that in defining the points on the transfer characteristics from the drain characteristics, only the saturation levels are employed, thereby limiting the region of operation to levels of V_{DS} greater than the saturation levels as defined by Eq. (5.12).

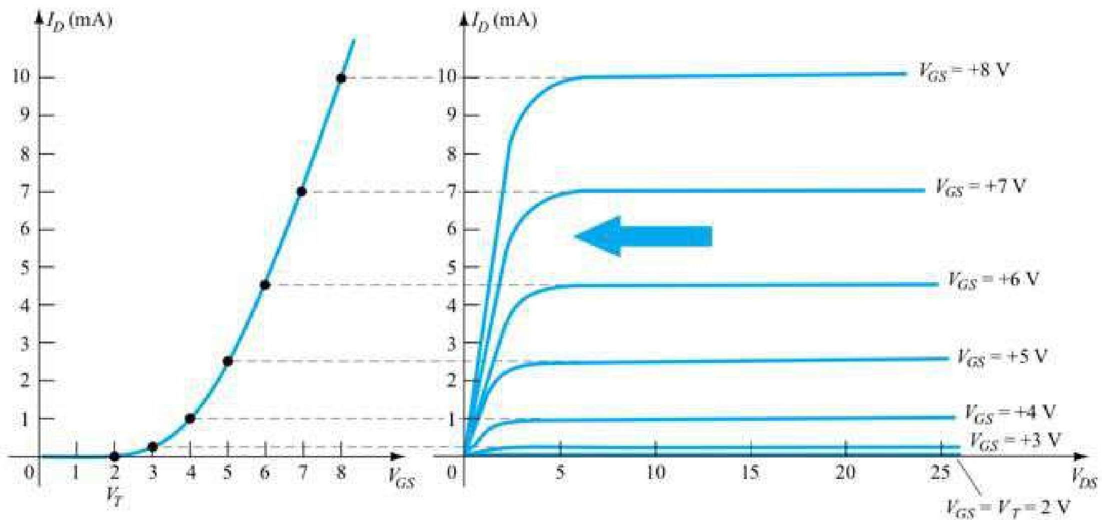

Figure 5.35 Sketching the transfer characteristics for an *n*-channel enhancement-type MOSFET from the drain characteristics.

The transfer curve of Fig. 5.35 is certainly quite different from those obtained earlier. For an *n*-channel (induced) device, it is now totally in the positive V_{GS} region and does not rise until $V_{GS} = V_T$. The question now surfaces as to how to plot the transfer characteristics given the levels of k and V_T as included below for a particular MOSFET:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2$$

First, a horizontal line is drawn at $I_D = 0$ mA from $V_{GS} = 0$ V to $V_{GS} = 4$ V as shown in Fig. 5.36a. Next, a level of V_{GS} greater than V_T such as 5 V is chosen and substituted into Eq. (5.13) to determine the resulting level of I_D as follows:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2$$
$$= 0.5 \times 10^{-3}(5\text{ V} - 4\text{ V})^2 = 0.5 \times 10^{-3}(1)^2$$
$$= \mathbf{0.5\ mA}$$

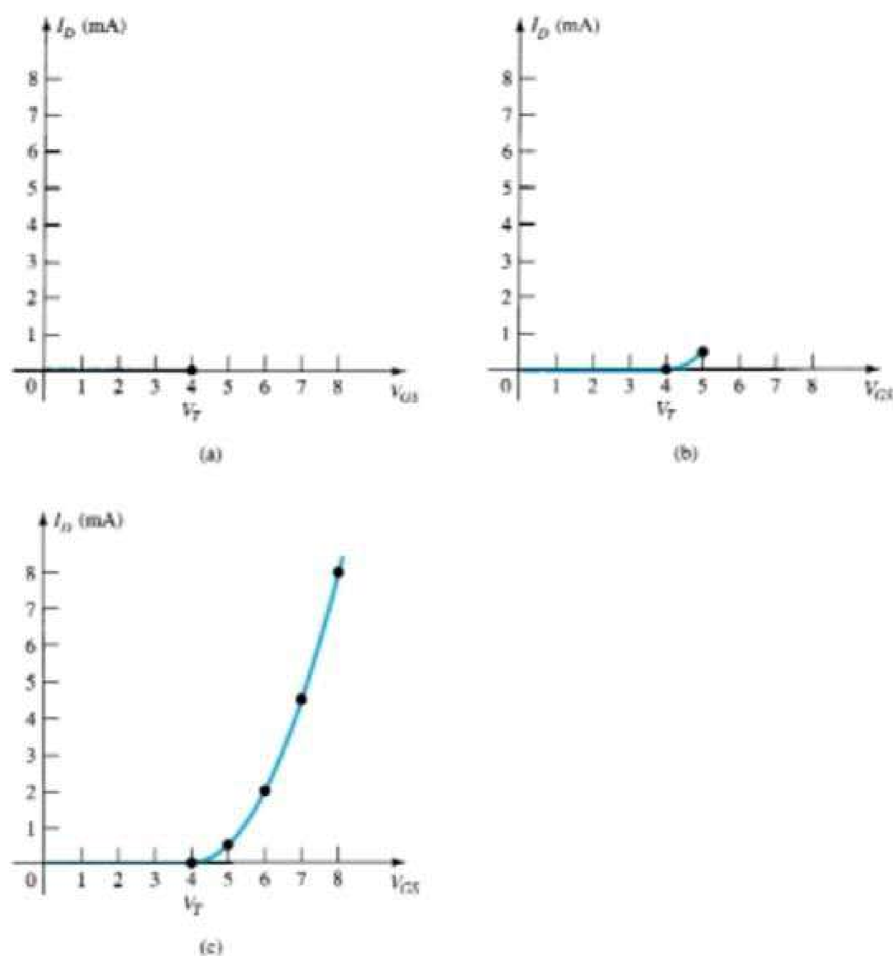

Figure 5.36 Plotting the transfer characteristics of an n-channel enhancement-type MOSFET with $k = 0.5 \times 10^{-3}$ A/V^2 and $V_T = 4$ V.

and a point on the plot is obtained as shown in Fig. 5.36b. Finally, additional levels of V_{GS} are chosen and the resulting levels of I_D obtained. In particular, at $V_{GS} = 6$, 7, and 8 V, the level of I_D is 2, 4.5, and 8 mA, respectively, as shown on the resulting plot of Fig. 5.36c.

p-Channel Enhancement-Type MOSFETs

The construction of a p-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 5.31, as shown in Fig. 5.37a. That is, there is now an n-type substrate and p-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 5.37c, with increasing levels of current resulting from increasingly negative values of V_{GS}. The transfer characteristics will be the mirror image (about the I_D axis) of the transfer curve of Fig. 5.35, with I_D increasing with increasingly negative values of V_{GS} beyond V_T, as shown in Fig. 5.37b. Equations (5.11) through (5.14) are equally applicable to p-channel devices.